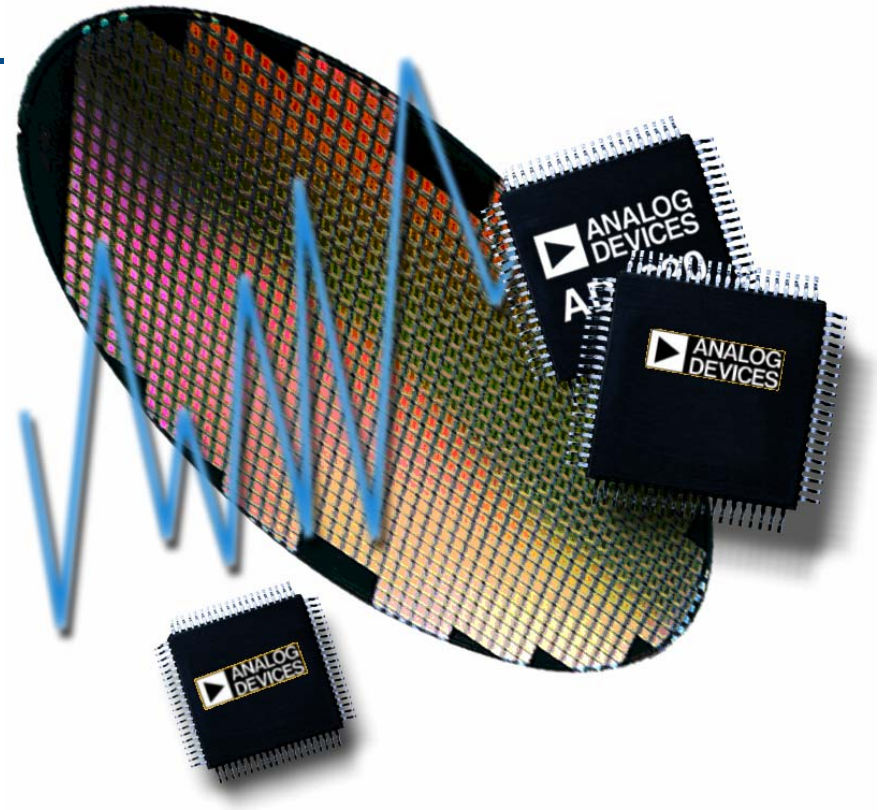

Reliability Report

Report Title: ADE7169 New Product

Report Number: 5477

Date: 2/20/2008

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Summary

This report documents the successful completion of the reliability qualification requirements for release of the ADE7169 product in a 64-LFCSP and 64-LQFP at STATS. The ADE7169 integrate Analog Devices, Inc., energy (ADE) metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, an RTC, an LCD driver, and all the peripherals to make an electronic energy meter with an LCD display in a single part.

This Qualification will cover the release requirement for the following products from the same family: ADE7566, ADE7569 and ADE7166.

ADE7169 Product Characteristics

Device	ADE7169
Maximum Power Dissipation (W)	0.014
Device / Die ID	ADE7169
Die Size (mm)	2.98 x 2.98
Wafer Fabrication Site	TSMC Fab - 3C
Wafer Fabrication Process	0.25um 2P4M w/EEPROM, 85A
Transistor Count	596668
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Polyimide Layer	Yes
Package/Assembly	
Available Package(s)	64-LQFP
Body Size (mm)	10.00 x 10.00 x 1.40
Assembly Location	STATS
Die Attach	Ablestik 8361J
Lead Frame Material	Copper
Bond Wire Type	Gold MKE-UB
Bond Wire Dia. (mils)	1.00
Mold Compound	Sumitomo 7372
Lead Finish	Tin Plate
Die Overcoat	NA
Lead Frame Supplier	
Moisture Sensitivity Level	3
Maximum Peak Reflow (°C)	260

Device	ADE7169
Maximum Power Dissipation (W)	0.014

Device / Die ID	ADE7169
Die Size (mm)	2.98 x 2.98
Wafer Fabrication Site	TSMC Fab - 3C
Wafer Fabrication Process	0.25um 2P4M w/EEPROM, 85A
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu
Polyimide Layer	Yes

Package/Assembly

Available Package(s)	64-LFCSP
Body Size (mm)	9.00 x 9.00 x 0.85
Assembly Location	STATS
Die Attach	Ablestik 8290
Lead Frame Material	Copper Olin 194
Bond Wire Type	Gold MKE-UB
Bond Wire Dia. (mils)	1.00
Mold Compound	Sumitomo G700E
Lead Finish	Tin Plate
Mold Compound	NA
Lead Finish	Gold
Lead Frame Supplier	
Moisture Sensitivity Level	3
Maximum Peak Reflow (°C)	260

Package/Assembly Qualification Test Results

The below table provides a description of the Assembly/Package qualification tests conducted and the associated test results on the ADE7169 and other products manufactured on the same technologies as described in the product characteristics table.

Test Name	Conditions	Specification	Device	Package	Lot #	Sample Size	Qty. Rejects
Autoclave	121C 100%RH 2atm P168	JEDEC-STD-22, Method A102	AD5383	100-LQFP	f156005.4	44	0
			AD5390	64-LFCSP	f155757.5	11	0
			AD5391	64-LFCSP	f156012.7	11	0
			AD5392	64-LFCSP	f155760.4	11	0
			AD6533	64-LFCSP	f156268.3	45	0
					f156268.4	45	0
					f156269.3	45	0
					f156269.6	45	0
					f156270.3	44	0
					f156270.4	45	0
			AD80076	64-LQFP	Q4020.5	45	0
					Q4020.6	45	0
					Q4020.7	45	0
			ADV7300A	64-LQFP	f155335.3	45	0
					f155336.3	32	0
					f155337.3	32	0
	121C 100%RH 2atm P96	JEDEC-STD-22, Method A102	ADE7169	64-LQFP	Q5477.26	32	0
					Q5477.27	32	0
					Q5477.28	32	0
HTS	150C P1000	JEDEC-STD-22, Method A103	AD5380	100-LQFP	f155832.3	45	0
SHR	See MSL CSAM POST	ADI-0049	AD6533	64-LFCSP	f156268.7	11	0
					f156269.8	11	0
					f156270.7	11	0
					f156270.8	11	0
			ADE7169	64-LFCSP	Q5477.24	30	0
			ADV7300A	64-LQFP	f155335.1	11	0
					f155336.1	45	0
					f155337.1	11	0
Temp Cycle	-55C/+125C P1000	JEDEC-STD-22, Method A104	AD5384	100-mBGA	f156869.5	30	0
	-65C/+150C P500	JEDEC-STD-22, Method A104	AD5381	100-LQFP	f156004.5	45	0
			AD5390	64-LFCSP	f155757.4	30	0
			AD5391	64-LFCSP	f156012.8	28	0
			AD5392	64-LFCSP	f155760.5	30	0
			AD6533	64-LFCSP	f156268.5	44	0
					f156268.6	45	0
					f156269.4	45	0
					f156269.5	45	0
					f156270.5	45	0
					f156270.6	45	0
			AD80076	64-LQFP	Q4020.10	45	0
					Q4020.8	45	0

Test Name	Conditions	Specification	Device	Package	Lot #	Sample Size	Qty. Rejects
					Q4020.9	45	0
			ADE7169	64-LQFP	Q5477.20	32	0
					Q5477.21	32	0
					Q5477.22	32	0
			ADV7300A	64-LQFP	f155335.2	45	0
					f155336.2	45	0
					f155337.2	43	0
Thermal Shock	-65C/+150C P500	JEDEC-STD-22, Method A106	AD5381	100-LQFP	f156004.4	45	0
			AD80076	64-LQFP	Q4020.11	45	0
			ADE7169	64-LQFP	Q5477.29	32	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260+0/-5ºC.

Samples of the many devices manufactured with these process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site

Process Qualification Test Results

The below table provides a description of the process qualification tests conducted and the associated test results on the ADE7169 and other products manufactured on the same technologies as described in the product characteristics table.

Test Name	Conditions	Specification	Device	Fab Process	Lot #	Sample Size	Qty. Rejects
Data Retention Bake	150C P1000	Per Data Sheet	ADUC7026	0.25um 2P4M w/EEPROM 100A	f158411.5	35	0
				0.25um 2P4M w/EEPROM 100A	f158421.5	32	0
	150C P500	Per Data Sheet	ADUC7026	0.25um 2P4M w/EEPROM, 85A	f157915.5	45	0
	225C P750	Per Data Sheet	ADE7169	0.25um 2P4M w/EEPROM, 85A	Q5477.7aa	35	0
					Q5477.8a	35	0
	85C P750	Per Data Sheet	ADE7169		Q5477.9A	35	0
ELF	125C P168	MIL-STD-883, Method 1015	ADUC7026	0.25um 2P4M w/EEPROM 100A	f158411.2	100	0
					f158421.10	100	0
EPROM Endurance Cycling	-40C, 10K cycles Single Duration	J-STD-22 Method A117	ADUC7026	0.25um 2P4M w/EEPROM 100A	f158509.5	35	0
	-40C, 20K Cycles Single Duration	J-STD-22 Method A117	ADE7169	0.25um 2P4M w/EEPROM, 85A	Q5477.11	35	0
					Q5477.4	35	0
					Q5477.5	35	0
					Q5477.6a	35	0
					Q5477.8	35	0
	125C, 10K Cycles Single Duration	J-STD-22 Method A117	ADUC7026	0.25um 2P4M w/EEPROM 100A	f158507.4	35	0
					f158508.5	35	0
					f158509.4	35	0
	25C, 10K Cycles Single Duration	J-STD-22 Method A117	ADUC7026		f158409.3	32	0
					f158409.9	32	0
					f158411.3	32	0
					f158421.5	32	0
					f158421.8	36	0
					f158508.4	35	0
	25C, 20K Cycles Single Duration	J-STD-22 Method A117	ADE7169	0.25um 2P4M w/EEPROM, 85A	Q5477.12	35	0
					Q5477.7	35	0
					Q5477.9	35	0
			ADUC7026	0.25um 2P4M w/EEPROM, 85A	f157915.5	55	0
HAST	130C 85%RH	JEDEC-STD-22,	ADE7169	0.25um 2P4M	Q5477.1	32	0
					Q5477.2	32	0

Test Name	Conditions	Specification	Device	Fab Process	Lot #	Sample Size	Qty. Rejects
	2atm, Biased P96	Method A110		w/EEPROM, 85A	Q5477.3	32	0
HTOL	125C<Tj<135C, Biased P2000	JESD22-A108	AD80028	0.25um DPQM CMOS	R7218	45	0
					R7219	45	0
					R7220	45	0
			ADE7169	0.25um 2P4M w/EEPROM, 85A	Q5477.10a	32	0
					Q5477.11a	32	0
					Q5477.12A	32	0
	135C<Tj<150C, Biased P1000	JESD22-A108	ADUC7026	0.25um 2P4M w/EEPROM 100A	f158409.9	32	0
					f158411.8	32	0
					f158421.8	32	0
LTS	-20C P2000		AD80028	0.25um DPQM CMOS	R4951.2	15	0
					R4951.3	15	0
					R4951.4	15	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260+0/-5ºC.

Samples of the many devices manufactured with these process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site

ESD Test Results

The results of ESD testing is summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed in the above table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/world/quality/manuals/.

Table 4: ADE7169 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	64-LQFP	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	500V	1000V	C4
HBM	64-LQFP	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	1500V	2000V	1C

Latch-Up Test Results

Six samples of the ADE7169 passed Latch-up testing at Ta=25ºC per JEDEC Standard JESD78, Class I.

Approvals

Reliability Engineer: Arnaud Sow
This report has been approved by electronic means (3.6).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page:	http://www.analog.com
Sales Info:	http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data:	http://www.analog.com/world/quality/read/1stpage.html
Reliability Handbook:	http://www.analog.com/corporate/quality/manuals/